REMARKS

This Amendment is submitted in response to the Office Action dated October 6, 2003, having a shortened statutory period set to expire January 6, 2004, extended to February 6, 2004.

Applicant notes upon review of the present Office Action that the Change of Correspondence Address filed July 16, 2002, and received by the USPTO on July 22, 2002, has not been entered. Applicant respectfully requests the Examiner to correct the correspondence address.

Next, in paragraph 3 of the present Office Action, Claims 3 and 10 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 3 and 10 of copending U.S. Patent Application Serial No. 09/598,435. In response, Applicant offers to submit a terminal disclaimer to obviate this rejection in the event that the copending application issues.

Next, in paragraph 5 of the present Office Action, Claims 1-23 are rejected under 35 USC § 103(a) as unpatentable over U.S. Patent No. 5,913,048 to *Glew et al.* (*Glew*) in view of U.S. Patent No. 6,360,314 to *Webb, Jr. et al.* (*Webb*). That rejection is respectfully traversed, and favorable reconsideration of the claims is requested.

The combination of *Glew* and *Webb* does not render the present invention unpatentable under 35 U.S.C. § 103 because that combination does not teach or suggest each feature recited in the present claims. For example, the combination of *Glew* and *Webb* does not teach or suggest, "queue management logic that, responsive to execution of a second load instruction, detects by reference to said load queue whether a data hazard exists, and if so, outputs said load data retrieved by said first load instruction from said entry to said register set in accordance with said second load instruction," as recited in exemplary Claim 1.

With respect to the above feature of Claim 1, the Examiner, in paragraph 7 of the present Office Action, notes that *Glew* does not teach or suggest the claimed "queue management logic." Indeed, *Glew* explicitly teaches at col. 6, lines 63-65 that a data hazard occasioned by a remote

processor writing a speculatively read location causes "the load and subsequent operation [to be] cleared and reexecuted to retrieve the correct data." Thus, *Glew* not only fails to disclose the claimed "queue management logic," but also explicitly teaches against Applicant's claimed technique of utilizing "load data retrieved by said first load instruction" and buffered within a load queue to satisfy the transfer of data into a register set indicated by a second load instruction.

Because *Glew* does not disclose and, in fact, teaches against the claimed "queue management logic," the Examiner then cites col. 1, line 66 through col. 2, line 15, col. 4, lines 43-48, and col. 7, lines 61-63 of *Webb* as teaching the claimed "queue management logic." In relevant part, the cited passages teach that *Webb* solves the problem of a load instruction failing to load the data written by an earlier store instruction by providing:

> ... a bypass mechanism that compares the address of each load instruction with a set of recent stores that have not yet updated memory. A match of the recent stores provides the desired load data instead of having to retrieve the data from memory.

Webb, col. 4, lines 44-48. In other words, *Webb* teaches the use of store data from a store queue to satisfy a load operation indicated by a load instruction. Claim 1, in contrast, recites the use of load data within a load queue retrieved by a first load instruction to satisfy a load operation indicated by second load instruction. Clearly, the use of store data to correct an instruction ordering problem as taught by the Examiner's combination of *Webb* and *Glew* does not teach or suggest the use of load data to address a data hazard as recited in exemplary Claim 1.

Furthermore, the queue management logic of the present invention would not have been obvious to those skilled in the art at the time of the present invention in view of the combination of *Glew* and *Webb*. Store queues, such as that disclosed by *Webb*, are required to buffer store data of a store operation until the indicated store is actually performed in memory (e.g., a data cache). It is therefore logical that *Webb* utilizes the stored data to satisfy a load operation, given the fact that the data in the store queue must be accessible and it is desirable, for correctness, that a load operation receives the newest data rather than the potentially stale data stored within the data cache.

However, this same reasoning is not applicable to the load queue and associated queue

management logic recited in the present claims. Conventional load queues do not buffer load data and the contents of conventional load queues are not accessible by other instructions. Moreover, there is no teaching in any reference of record regarding the use of load data retrieved by one load instruction to satisfy another load instruction. Consequently, if a person of ordinary skill in the art at the time of the present invention, for example, an integrated circuit designer or architect, had before him the teachings of *Glew* and *Webb*, the present invention would not have been obvious because the cited references would offer no teaching or suggestion to modify the teachings of *Glew* and *Webb* with respect to a store queue and somehow apply those teachings to a load queue and associated queue management logic to obtain the invention recited in the present claims.

Because the combination of *Glew* and *Webb* does not teach or suggest, "queue management logic that, responsive to execution of a second load instruction, detects by reference to said load queue whether a data hazard exists, and if so, outputs said load data retrieved by said first load instruction from said entry to said register set in accordance with said second load instruction," Applicant respectfully submit that exemplary Claim 1, similar Claims 8 and 16, and their respective dependent claims are not rendered unpatentable by the combination of *Glew* and *Webb* under 35 U.S.C. § 103.

Having now addressed each rejection set forth in the present claims, Applicant respectfully submits that all pending claims are in condition for allowance and respectfully requests such allowance.

Enclosed is a check in the amount of $110.00 for a one-month extension of time. No additional fee or extension of time is believed to be required; however, in the event any fee, including a fee for an extension of time, is required, please charge that fee to IBM Deposit Account No. **09-0447**.

Respectfully submitted,

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